SIMULATING "LARGE" MICROWAVE CIRCUITS WITH THE PARALLEL PLANAR GENERALIZED YEE ALGORITHM

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ABSTRACT

The Planar Generalized Yee (PGY) algorithm is presented for the full-wave analysis of "electrically-large" grounded co-planar (GCPW) circuits. The method has a significant advantage over traditional Yee-algorithm based finite-difference time domain (FDTD) methods in that it is based upon unstructured and irregular grids. The PGY algorithm has been efficiently implemented on massively parallel computers and is ideal for the rapid, broadband analysis of packaged, large, high-density circuits and multi-chip modules (MCM's). Simulation and measured results on several "electrically-large" circuit structures are presented.

INTRODUCTION

Multi-function microwave monolithic integrated circuit technology has greatly expanded component, subsystem and system architecture design options. Multichip module (MCM) assemblies offer unparalleled performance capabilities while at the same time have proliferated in complexity. As a result, the component, circuit and package design process demands comprehensive, rapid and accurate "packaged" MCM 3D electromagnetic (EM) simulation and analysis. EM simulation software that enables designers to quickly optimize their designs allows the design team to assess circuit and package performance early in the design process while design changes are relatively inexpensive.

In this paper, we present the Planar Generalized Yee (PGY) simulation and the measured results of circuit structures often found in the design of microwave transmit/receive (T/R) modules and communication MCM's.

The Generalized Yee algorithm is based upon the discretization of Maxwell's equations in their integral form by projecting the vector fields onto the edges of a dual staggered grid. Unlike traditional FDTD approaches, the grid is assumed to be unstructured and irregular. The Planar Generalized Yee method was developed from recognizing that a large class of microwave circuits are predominantly planar. Such circuits have detailed features in the x-y plane and only interconnecting vias in the z-dimension. Only a two-dimensional grid needs to be stored in the PGY method. This greatly reduces the memory requirement of the Generalized Yee algorithm.

The analysis of single component circuits can typically be modeled on conventional workstations or sequential computers in reasonable amounts of time. On the other hand, the analysis of multi-component circuits requires greater resources. It is becoming more evident that distributed parallel computing is a highly cost-effective means of achieving supercomputing performance. The PGY algorithm is well suited for such high performance distributed memory computing.

The PGY code outputs key circuit design parameters: S parameters, characteristic impedance, phase velocity and both static and animated vector field plots. These capabilities coupled with the implementation of the PGY algorithm on massively parallel computers make this methodology very well suited for the broadband performance evaluation of electrically large, high density, packaged MMIC chip assemblies and subsystems.

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SIMULATION PROCESS AND FEATURES

The PGY method [1-3] performs the discrete solution of the time-dependent Maxwell's equations in their integral form. Similar to the familiar FDTD method [4-5], it is based on an explicit time-marching solution scheme. The PGY algorithm utilizes unstructured, non-orthogonal grids. This provides more accurate modeling of detailed

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and curved planar circuit structures than staircasing approximations required by traditional FDTD methods. The grid is assumed to be unstructured in the transverse planes parallel relative to the layered media, and orthogonal along the normal axis (Figure 1). Exploiting the predominantly planar circuit features in this manner greatly conserves memory and improves the computational performance [2]. The use of a grid that is unstructured in two dimensions and consists of cells of varying shapes and sizes can easily be space-fitted to uniquely-shaped structures in the circuit topology. Unstructured grids provide linear approximations of irregular edges, e.g., circular vias, and easily conforms to irregular geometries. Regions that require higher resolution to capture the field behavior can be modeled by locally dense grids, while regions where the field varies slowly are modeled by coarser grids.

The PGY simulation process, detailed in Figure 2, is interfaced with a commercial CAD software package SDRC-IDEAS®. The CAD software is used to design and build the circuit models. It is also used to generate the two-dimensional unstructured mesh via automatic grid generation techniques. The node-based two-dimensional mesh is subsequently partitioned on the workstation using spatial-decomposition algorithms. Since the generation of the meshes of very large models can be extremely time-consuming and memory intensive, an automatic mesh refinement technique has been implemented in the parallel algorithm.

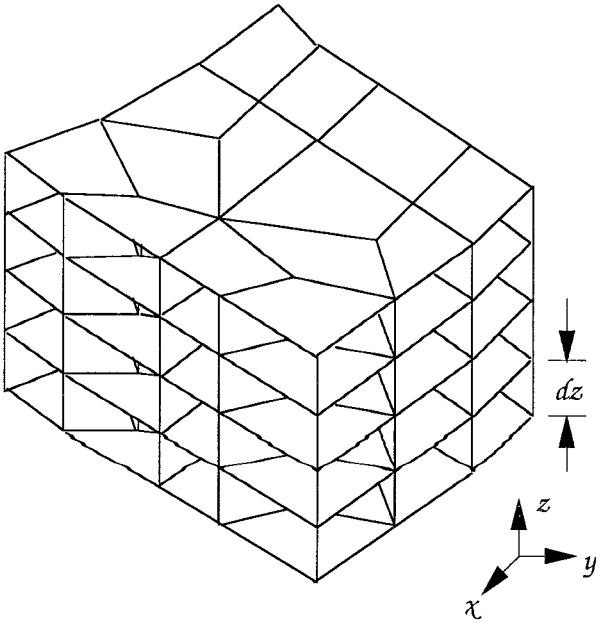

Figure 1. Planar Generalized Yee algorithm lattice composed of an unstructured grid in the transverse planes and a regular grid in the z-direction

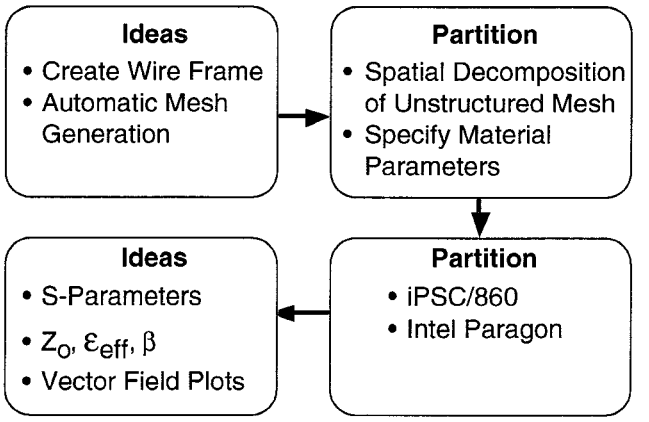

Figure 2. Flow diagram of the PGY simulation process

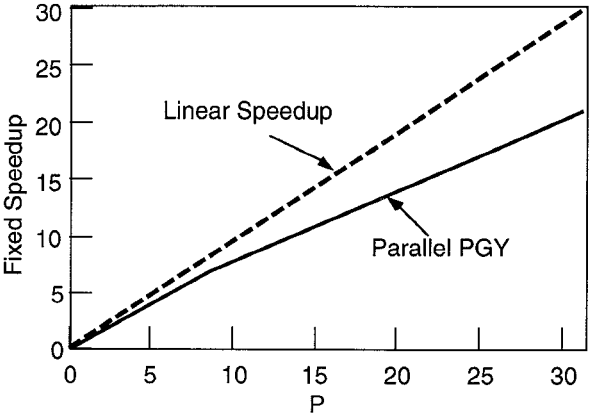

Figure 3. Fixed Speedup of the parallel PGY algorithm over 32 processors of the Intel iPSC/860

The parallel PGY algorithm is based on a spatial decomposition of the unstructured mesh into equal sized non-overlapping subdomains. Due to the explicit nature of the time-domain solution, it is highly scalable. In Figure 3, the speed-up of a fixed problem size over 32 processors recorded on an Intel iPSC/860 multi-processor computer is compared to the ideal linear speedup.

TEST CIRCUIT AND MEASUREMENT DESCRIPTION

Abrupt and tapered GCPW to microstrip circuit transitions, shown in Figures 4 and 5, were selected for simulation and measurement. Figure 6 illustrates the cross section of a GCPW circuit printed on a 25 mil thick alumina substrate. The 50 Ohm line impedance circuits were fabricated on 1 inch by 0.5 inch by 25 mil thick alumina substrates with a thick film process. Five mil gaps separate the 10 mil wide center conductor from the ground return strips. The GCPW ground return strips were connected to the bottom-side ground plane with

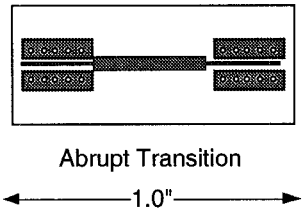

Figure 4. GCPW Abrupt Junction Transition Geometry

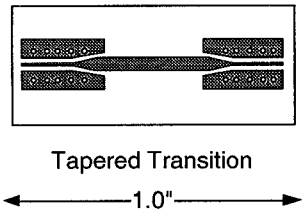

Figure 5. GCPW Tapered Junction Transition Geometry

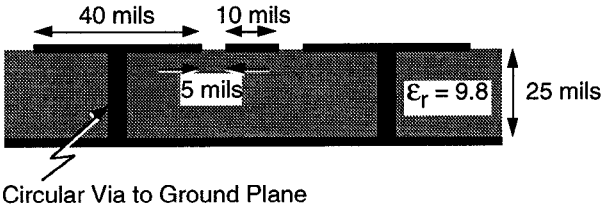

Figure 6. Cross Section of 50 Ω Grounded CoPlanar WaveGuide (GCPW) printed on a 25-mil alumina substrate

6 mil diameter conducting vias located at the centerline of the strips and spaced every 50 mils. Ten substrates of each circuit type were fabricated. Three substrates of each type were selected at random for measurement.

Ground-signal-ground microwave wafer probes were used with an HP 8510 automatic network analyzer (ANA) to measure the circuit 2-port S parameters. Data was collected from 2-18 GHz at 100 MHz frequency intervals. The probe tips contacted the circuits ~ 2 mils inside the GCPW line end. The ANA was calibrated with an alumina substrate standard that contained CPW short circuit, matched load and through line artifacts.

Data from the 3 substrates per circuit type exhibited good repeatability. $|S_{12}|$ varied by no more than ± 0.25 dB while $|S_{11}|$ varied by ± 3 dB @ -30 dB level.

SIMULATION AND MEASUREMENT COMPARISON

Figure 7 compares the measured and simulated scattering parameters for the abrupt junction. The simulation results agree well with the measured results.

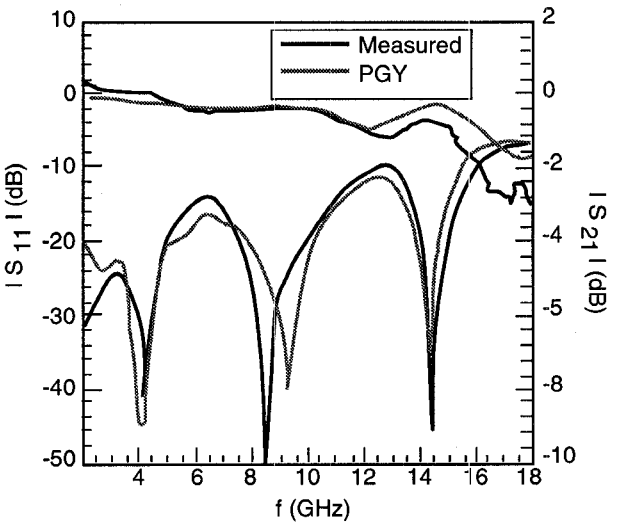

Figure 7. Comparison of measured and PGY results for S_{11} and S_{21} for an abrupt junction circuit with vias

PGY predicts the maximum and minimum insertion loss of this circuit. The resonant frequencies near 4 GHz, 8.5 GHz, and 14 GHz frequencies predicted by PGY are slightly shifted from the measured resonances. There is about a 1 dB difference in the simulated and measured S_{11} at the higher frequencies. The simulations did not incorporate any dielectric or conductor losses, while the dielectrics and conductors of the fabricated circuits had material losses. The PGY model used symmetric octagonal-shaped vias, while the vias in the fabricated circuits had the typical manufacturing imperfections and irregularities.

Figure 8 compares the measured and simulated results for the tapered junction circuit. The overall behavior of this circuit is predicted by the PGY simulation. There are some differences in the location of the predicted and measured resonances below 10 GHz. PGY predicts the maximum and minimum insertion loss. This circuit shows some difference between the predicted and measured return loss at the higher frequencies. Similar type of return loss behavior has been observed for GCPW [6-7] and CPW [8]. Further characterization of these effects can be easily accomplished by the visualization of time-history plots of the EM fields.

The simulation of the circuits required about 6 million unknowns. The structure was excited by a broad-band Gaussian pulse and required 30,000 time iterations to reach steady state. This took approximately 2 hours on 32 nodes of the Intel iPSC/860. Similar simulations using commercial codes based upon frequency domain techniques would have taken days. Typical simulations on the Intel Delta over P processors requires run times on the order of $(N_{unknowns} \times N_{iterations}/S(P)) \times 0.13 \times 10^{-6}$ seconds, where $N_{unknowns}$ is the number of unknowns, $N_{iterations}$ is the number of time iterations, and S(P) is the expected speed-up shown in Figure 3.

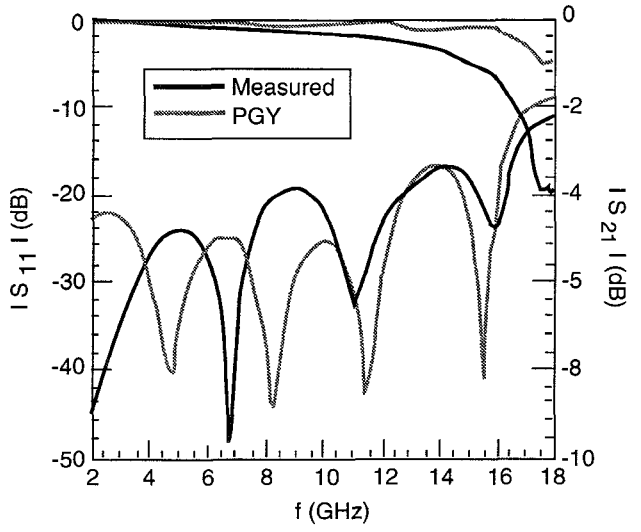

Figure 8. Comparison of measured and PGY results for S_{11} and S_{21} for the tapered junction circuit with vias

CONCLUSIONS

The PGY code, running on massively parallel processors, is well suited for simulating and analyzing electrically-large, high density multichip RF and microwave packaged and open circuit structures. The code demonstrated its ability to predict the S parameter performance of the selected "electrically-large" test circuits that contained curved conductors.

Rapid simulation time enables the designer to conduct necessary tradeoffs and design refinements. As a result, the designer will have the ability to confidently explore and optimize new architectures built around the latest MMIC chip technology. This includes "stacked" 3-dimensional MCM packaged assemblies which contain dense, RF, control and power interconnections and interfaces.

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